IN THE CLAIMS:

Please AMEND claim 40, as follows. For the Examiner's convenience, all claims currently pending in this application have been reproduced below:

1-39. (Canceled)

40. (Currently Amended) A method of cutting a substrate on which two-dimensionally arranged semiconductor elements are installed, said method comprising the steps of:

cutting ~~at least~~ a slice line provided on the substrate while detecting a misalignment of a cutting position from the slice line and correcting the cutting position;

cutting the substrate on a side opposing the slice line without correcting a cutting position on the side opposing the slice line; and

electrically checking, after the cutting step is completed, a monitor line, comprising an electrical conductor and provided on the substrate between the slice line and an adjacent one of the semiconductor elements installed.

41. (Previously Presented) The method according to claim 40, wherein the substrate is fixed on a stage having a groove corresponding to the slice line to cut the substrate.

42. (Previously Presented) The method according to claim 40, further comprising providing a guide line on the substrate and wherein the step of detecting a misalignment of the cutting position is performed by using the guide line.

43. (Previously Presented) The method according to claim 40, wherein the slice line comprises an electrode layer constituting the semiconductor element.

44. (Previously Presented) A method of cutting a substrate on which two-dimensionally arranged semiconductor elements are installed, said method comprising the steps of:

detecting a guide line provided at an area which interposes a semiconductor element and opposes a slice line provided at a cutting position of the substrate;

cutting the substrate along the slice line while correcting a cutting position based on the detected guide line.

45. (Previously Presented) The method according to claim 44, wherein the guide line is cut after the substrate is cut along the slice line.

46. (Previously Presented) A method of cutting a substrate on which two-dimensionally arranged semiconductor elements are installed, said method comprising the steps of:

cutting the substrate along a slice line provided at a cutting position of the substrate;

detecting, during the cutting of the substrate, a guide line provided at an area which interposes a semiconductor element and opposes the slice line, the guide line being provided corresponding to the slice line, to detect misalignment; and

cutting the substrate while correcting the misalignment.

47. (Previously Presented) A substrate on which two-dimensionally arranged semiconductor elements are installed, said substrate comprising:

a slice line provided at a cutting position on the substrate; and

a guide line provided for detecting the cutting position on the substrate,

wherein the guide line is provided at an area which interposes a semiconductor element and opposes the slice line on the substrate.

48. (Previously Presented) The substrate according to claim 47, wherein the guide line comprises an electrode line which constitutes the semiconductor element and is provided on the substrate.

49. (Previously Presented) The substrate according to claim 47, wherein the slice line and the guide line comprise an electrode layer provided on the substrate.

50. (Previously Presented) The substrate according to claim 49, wherein the electrode layer is formed by a same material as that of an electrode line constituting the semiconductor element provided on the substrate.

51. (Previously Presented) An apparatus for cutting a substrate on which two-dimensionally arranged semiconductor elements are installed, said apparatus comprising:

cutting means;

moving means for relatively moving the cutting means with respect to the substrate;

position detecting means for detecting a cutting position of the substrate; and

adjusting means for adjusting the cutting position based on positional information by the position detecting means,

wherein the position detecting means detects a guide line provided at an area which interposes a semiconductor element and opposes a slice line provided at the cutting position, the guide line being provided corresponding to the slice line, thereby detecting the cutting position.